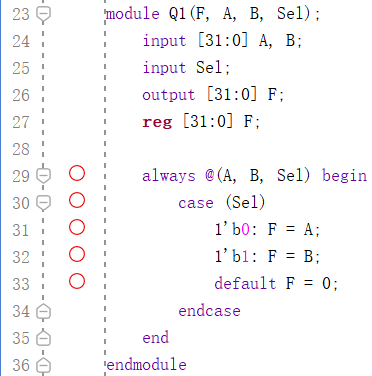
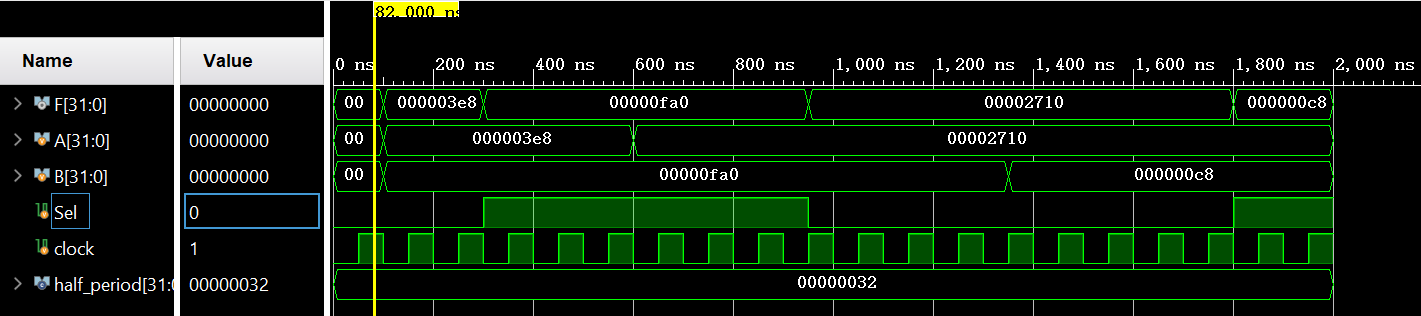
**HW5 Report**

Q1.

Verilog Code:

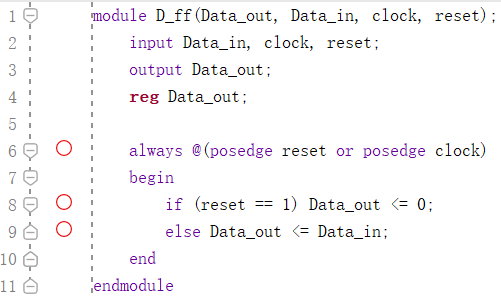


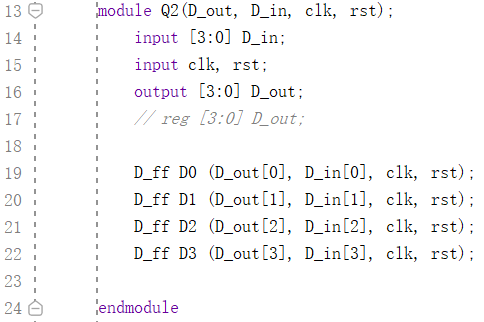
Simulation Result:



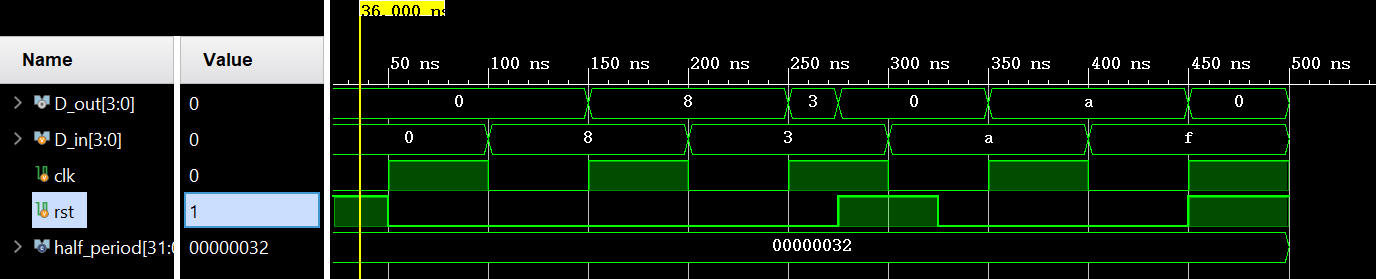
Q2.

Verilog Code:



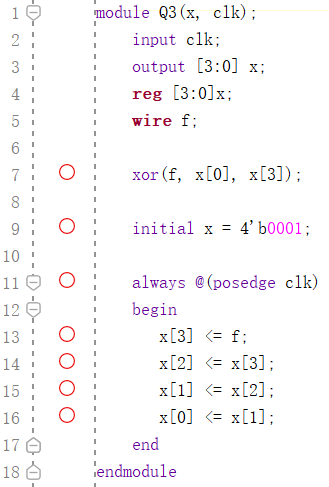


Simulation Result:

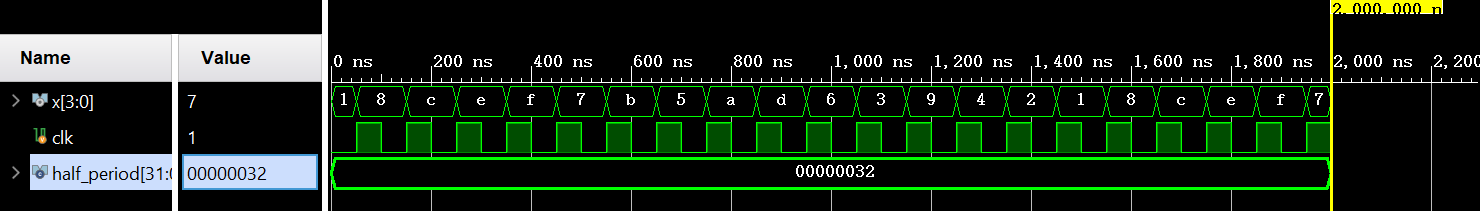


Q3.

Verilog Code:

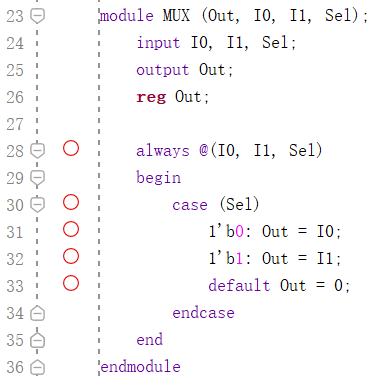


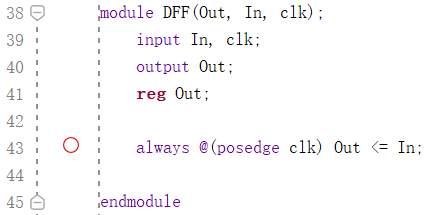
Simulation Result:

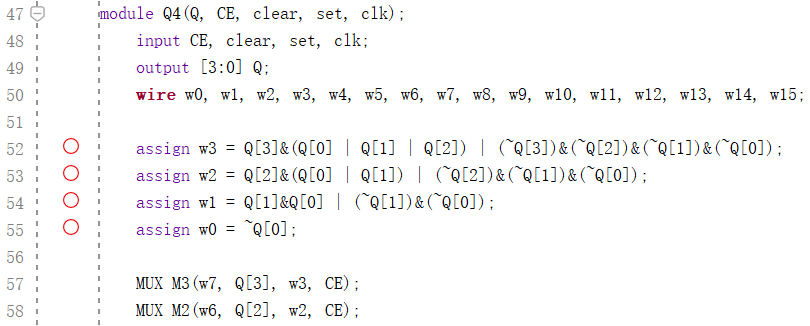


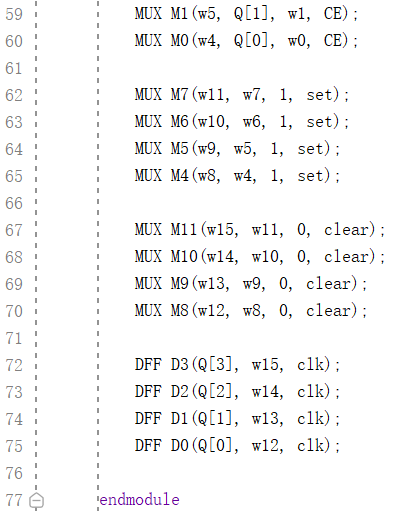
Q4.

Verilog Code:

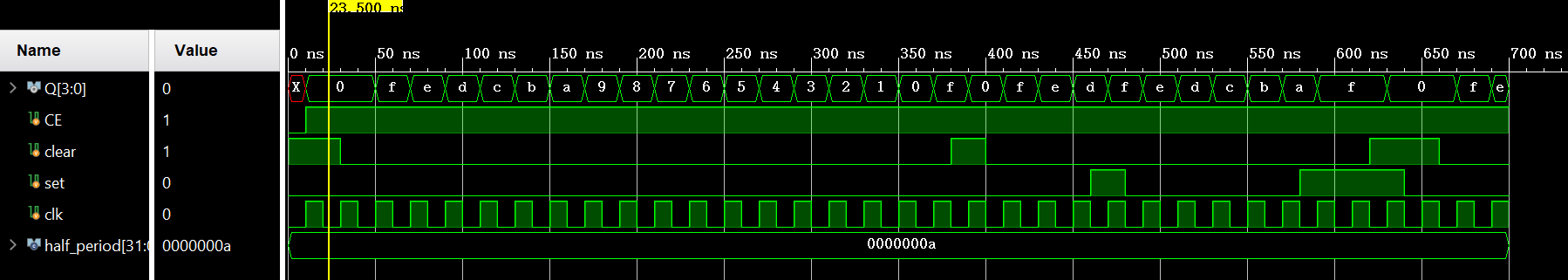






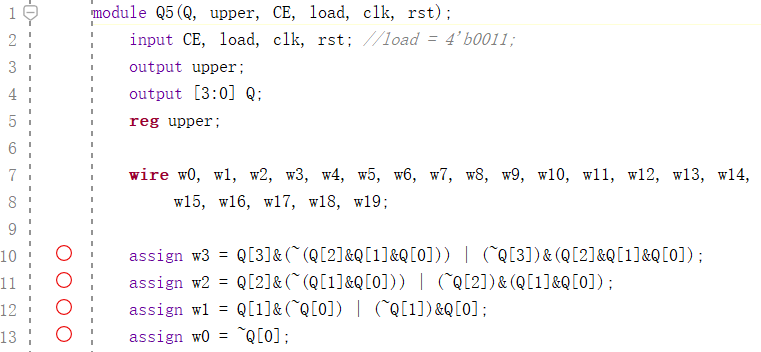


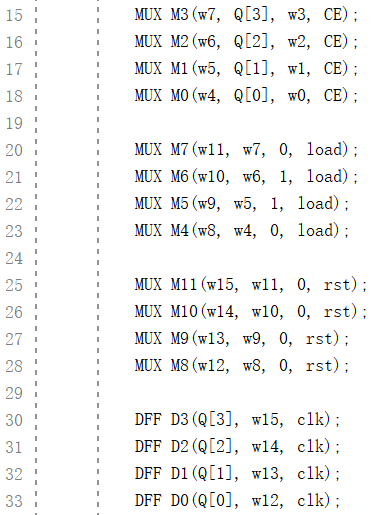
Simulation Result:

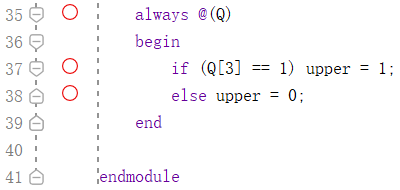


Q5.

Verilog Code:







Simulation Result:

